Temperature Impact on the *In-Situ* *S*-Parameter Calibration in Advanced SiGe Technologies

Andrej Rumiantsev [1), 2)]
[1)] MPI Corporation,
Chu-Pei City, Hsinchu County, Taiwan
[2)] Brandenburg University of Technology (BTU),
Cottbus-Senftenberg, Cottbus, Germany
a.rumiantsev@ieee.org

Ralf Doerner
Ferdinand-Braun-Institut (FBH),
Leibniz-Institut fuer Hoechstfrequenztechnik,
Berlin, Germany
ralf.doerner@fbh-berlin.de

Falk Korndoerfer
Innovations for High Performance Microelectronics (IHP)
Leibniz-Institut fuer innovative Mikroelektronik,
Frankfurt (Oder), Germany
korndoerfer@ihp-microelectronics.com

***Abstract*—This paper analyzes the *in-situ* *S*-parameter multiline TRL and the transfer TMR calibration methods for the sensitivity to the thermal variation of electrical characteristics of calibration standards. The standards were realized in IHP's SG13 130 nm SiGe:C BiCMOS process. The measurement experiment was performed for the frequency range up to 110 GHz. We demonstrate that the calibration error caused by thermal instability of electrical characteristic of standards is in order of magnitude of the system drift error and, thus, negligible.**

Keywords—S-parameter calibration, device characterization, mm-wave measurements, BiCMOS.

I. Introduction

Increasing demand for more content, higher data transfer rates and cost reduction pushes the development of advanced SiGe technologies operating at mm-wave and sub-THz ranges. Optimization of device models over extremely wide frequency ranges and across multiple temperatures as well as verification of the results with highest level of accuracy and confidence becomes more and more challenging. Therefore, accurate and consistent *in-situ* *S*-parameter calibration procedures covering wide frequency and temperature ranges are the critical success factor for development of advanced SiGe technologies.

The state-of-the-art *in-situ* *S*-parameter calibration techniques for Silicon processes were reviewed in [1]. It recommended implementation of two comparable calibration concepts: 1) the probe-tip calibration performed on the commercially available Alumina substrate, followed by the advanced six-step de-embedding procedure, and 2) straightforward *in-situ* multiline Thru-Reflect-Line (TRL) or transfer Thru-Match-Reflect (TMR, also known as LRM+). However, [1] presented results for the room temperature only. Possible variation of electrical characteristics of calibration standards with the change of the measurement temperature, and, as a result, the accuracy of the over-temperature calibration remained unclear.

Later, the work in [2] addressed this topic for the first calibration concept. It proposed a method for accuracy analysis of the over-temperature probe-tip calibration. It was demonstrated that the temperature variation has a marginal impact on the electrical characteristic of the evaluated commercially available Alumina calibration standards. In this paper, we present the investigation results for the second calibration concept applying custom on-wafer standards and the multiline TRL and the transfer TMR. The objective of this work is to identify standards parameters that are most sensitive to the temperature variation as well as to propose a practical method for compensation of possible calibration error.

II. Analysis Method

Multiline TRL and TMR calibration methods differently define calibration reference impedance Z_{REF}. For the multiline TRL, the reference impedance is set to the characteristic impedance Z_{LINE} of the line standard. Assuming that the conductive loss of the microstrip-designed transmission line is negligible in the frequency range of interest, we calculated Z_{LINE} from the measured capacitance per unit length C' and propagation constant γ, as proposed in [3, 4]. Once Z_{LINE} is known, the calibration reference impedance can be transformed to the desired value of $Z_{REF} = 50\,\Omega$.

The Z_{REF} for TMR depends on the impedance of the match (load) as well as γ and Z_{LINE} of the thru. Therefore, multiline TRL and the transfer TMR may show different calibration residual error across the temperature range.

As it was already proposed in [2], the maximum error bounds for measured *S*-parameters of a passive device are a reliable figure of merit (FoM) of the calibration accuracy, calculated by the calibration comparison technique at given temperature. The benchmark calibration conditions were established by using pre-characterized temperature-dependent electrical properties of standards. The test calibration was performed at the test temperature, but using electrical models of standards extracted at the room temperature. Thus, the maximum error bounds can be calculated for each temperature point and calibration method used.

III. Experimental Setup

A. Calibration Standards

The test structures were realized in IHP's SG13 process. It is a 130 nm SiGe:C BiCMOS process with 5 thin and 2 thick aluminum metallization layers [5]. The top metallization layers have 2 µm and 3 µm thickness, respectively. Two types of bipolar transistors are available in the process. The high speed HBTs feature f_T/f_{MAX} of 240 GHz/330 GHz at a breakdown voltage BV_{CEO} of 1.7 V. The high voltage HBTs BV_{CEO} of 3.7 V with cut-off frequencies f_T/f_{MAX} of 50 GHz/130 GHz.

We designed test structures consisting of open, short, load, thru, and 10 microstrip lines (Fig. 1). Their lengths vary from 0.4 mm to 15.1 mm. The length ratio between two lines is always non-integer. We decided for microstrip lines to circumvent influences of substrate losses in the silicon wafer.

The signal line is designed in the topmost metallization layer (TM2) and the ground plane in the lowest (M1). The signal line is 15 µm wide. The ground plane has a width of 90 µm. The insulator between signal line and ground plane is 9.8 µm thick with a dielectric constant of $\varepsilon_r = 4.1$. The expected line impedance is about 50 Ω with that dimensions.

All structures are placed in GSG pads with 100 µm pitch. We added 65 µm feeding lines between contact pad and lines to allow a homogenization of the fields.

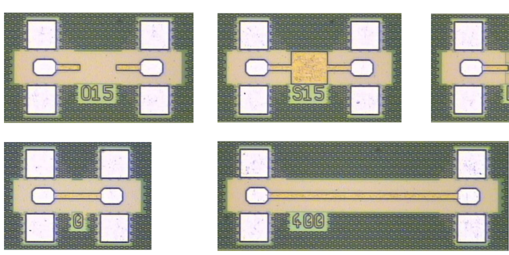

Fig. 1. Selected layouts of the designed calibration standards (from left to right: open, short, load, thru, and line).

B. Measurement Setup

The experimental setup included a semi-automatic thermal probe system PA200 and Agilent PNA 67 GHz vector network analyzer (VNA). Experiments were conducted for three temperature points: 233 K, 300 K, and 398 K covering typical device modeling temperature range. All measured data of calibration standards and the device under test were acquired uncorrected, in one series, and saved for further analysis. Thus, uncertainty caused by contact repeatability is minimized.

IV. Results and Discussion

First, the propagation constant γ (Fig. 2) and the capacitance per unit length C' were determined using the multiline TRL method for every temperature point. The extracted characteristic impedance of the line Z_{LINE} (Fig. 3), as well as other parameters of the calibration standards are given in the Table I.

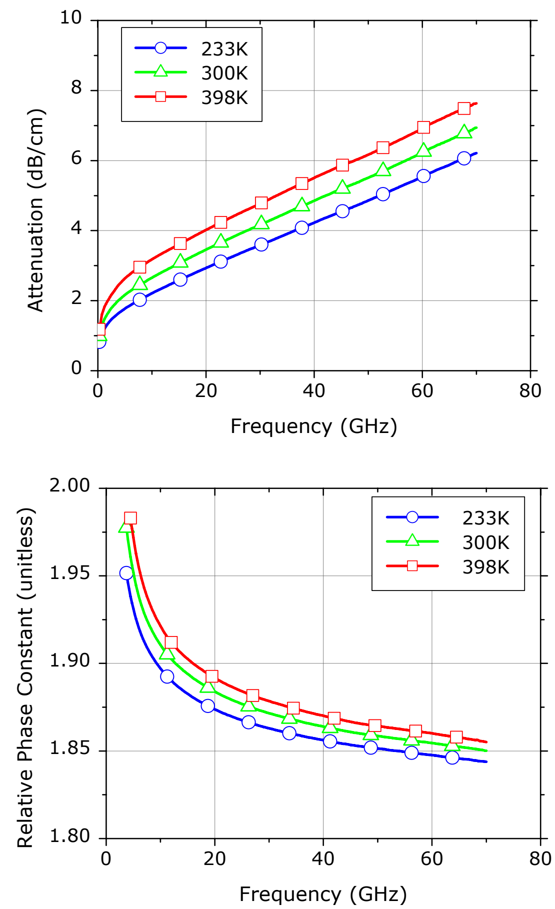

Fig. 2. Attenuation constant (top) and the relative phase constant (bottom) of the line standard measured across the temperature.

With the measurement temperature variation from 233 K to 398 K, the maximum variation of key standard parameters compared to room temperature (300 K) is: 1.8% for the load resistance, 33% for the M1 sheet resistance, 1.4% for the line capacitance per unit length C', 14% for the attenuation constant α, and is marginal (0.4%) for the relative phase constant β/β_0. As a result, the maximum variation of the characteristic impedance Z_{LINE} is 1.7% for its real and 15% for its imaginary part respectively (for 40 GHz frequency). We attributed measured variations in the electrical parameters of calibration standards to the temperature impact on the sheet resistance and the permittivity of dielectric. Once $Z_{LINE}(T)$, $R_{LOAD}(T)$ and $\gamma(T)$ are defined, the impact of each of them on the calibration accuracy of the multiline TRL and the transfer TMR can be estimated.

TABLE I. STANDARD PARAMETERS VARIATION OVER TEMPERATURE

Parameter	Temperature, K		
	233	*300*	*398*
α @ 40 GHz, dB/cm	4.22	4.85	5.53
β/β_0	1.856	1.864	1.870
C', pF/cm	1.248	1.241	1.224
$\Re(Z_{LINE})$ @ 40 GHz, Ω	49.61	50.10	50.96
$\Im(Z_{LINE})$ @ 40 GHz, Ω	-1.55	-1.79	-2.06
$R_{LOAD,P1}$, Ω	51.64	50.77	49.99
$R_{LOAD,P2}$ Ω	51.33	50.43	49.76
M1 sheet resistance, Ω/□	0.0835	0.1086	0.1439
TM2 sheet resistance, Ω/□	0.0082	0.0111	0.0151

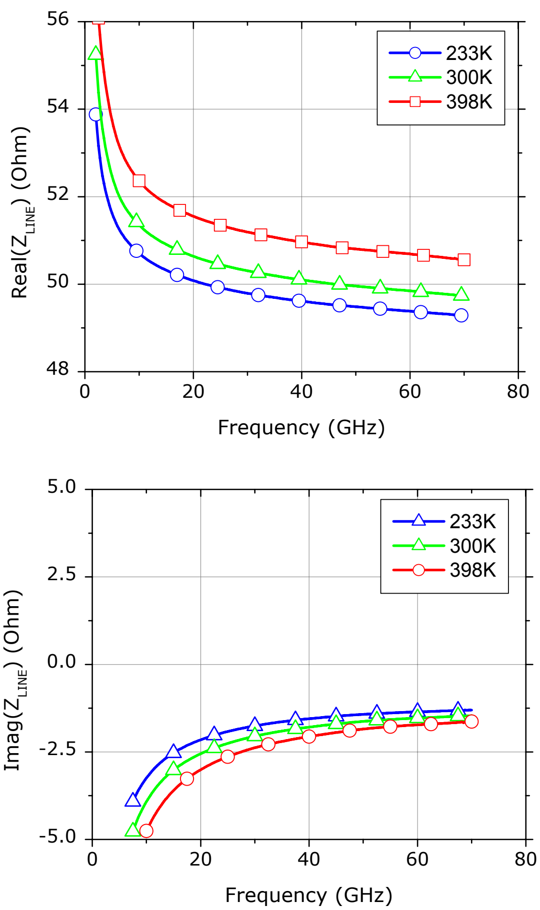

Fig. 3. Real (top) and imaginary (bottom) parts of the characteristic impedance Z_{LINE} of the line standard measured across the temperature.

We calculated the maximum error bounds for both calibration methods for simplified $(T = 300\,K)$ and characterized $(T = T_{TEST})$ models of calibration standards for every temperature point T_{TEST} using the method from [2]. The maximum error bounds are 0.02 for the multiline TRL for $T_{TEST} = 398\,K$ and 0.027 for the transfer TMR for $T_{TEST} = 233\,K$ at 67 GHz, respectively. It is lower than the typical drift of the on-wafer setup and, thus, negligible (Fig. 4). The setup drift was obtained from a separate experiment. Therefore, the extensive characterization of the electrical properties of both the lumped and the distributed calibration standards is not required. This founding significantly simplifies implementation of the over-temperature *in-situ* calibration for advanced SiGe technologies.

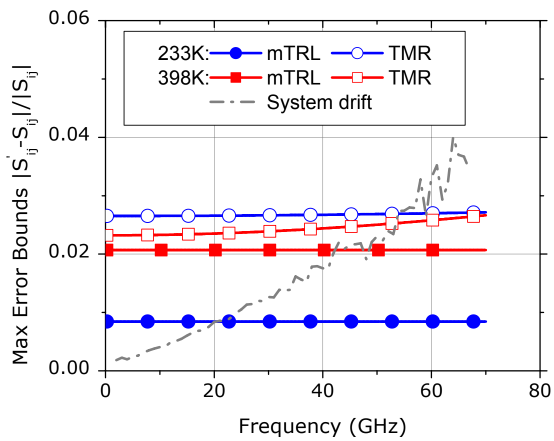

Fig. 4. Maximum error bounds calculated for multiline TRL, and transfer TMR for $T_{TEST} = 233\,K$ and $T_{TEST} = 398\,K$ with benchmark and worst case definition of standard properties. Typical experimental drift of a comparable setup is added for reference.

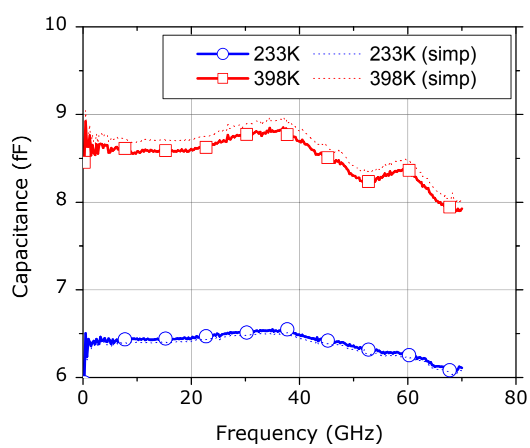

Fig. 5. C_{BE} of a test DUT extracted from the cold S-parameter conditions for the benchmark and simplified multiline TRL at $T_{TEST} = 233\,K$ and $T_{TEST} = 398\,K$. The results extracted for the transfer TMR are similar.

The calibration residual error of the simplified multiline TRL stems from the error of the characteristic impedance of the line ΔZ_{LINE} that we found to be frequency independent. Thus, we observed constant maximum error bound $|S'_{ij} - S_{ij}|/|S_{ij}|$. The transfer TRM residual errors are the sum of errors of the characteristic impedance ΔZ_{LINE} and the propagation constant $\Delta\gamma$ of the line, as well as of the impedance of the load ΔZ_{LOAD}. The individual impact of each of the errors depends on the frequency range: The error in the load resistance and the line characteristic impedance contribute the most at lower frequencies, while the impact of errors in the load reactance and line propagation constant predominate at higher frequencies.

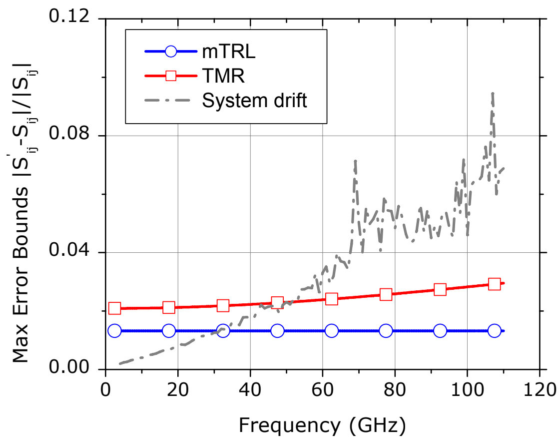

Fig. 6. Maximum error bounds calculated for multiline TRL, and transfer TMR for the 110 GHz setup and for $T_{TEST} = 358\,K$ with benchmark and worst case definition of standard properties. Typical experimental drift of a comparable setup is added for reference. Measurement data were obtained on the second experimental system.

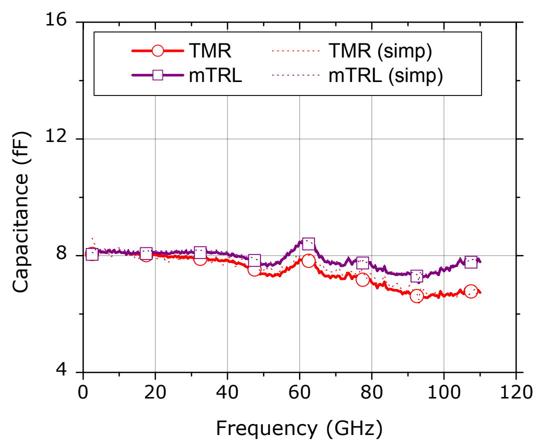

Fig. 7. C_{BE} of a test DUT extracted from the cold *S*-parameter conditions for the benchmark and simplified multiline transfer TMR at $T_{TEST} = 358\,K$. Measurement data were obtained on the second experimental system.

Finally, the capacitance C_{BE} of a test HBT at $T_{TEST} = 233\,K$ and $T_{TEST} = 398\,K$ was extracted from the cold S-parameters corrected with the benchmark and the simplified calibrations (Fig. 5). In both cases, the difference between the extracted value from the benchmark and the simplified calibration is negligible. Fig. 5 shows the results for the multiline TRL calibration. The results for the transfer TMR calibration are similar.

We repeated the experiment for the same device on a 110 GHz system, which allowed a temperature variation from 300 K to 358 K. The obtained results are, in general, comparable with those for the 67 GHz probe system (Fig. 6, 7). However, we observed a minor deviation of the extracted C_{BE} from the expected value above 60 GHz for the TMR calibration (up to 13% at 110 GHz). This error can be attributed to insufficiencies of the load standard model. It can be decreased by an appropriate description of the load impedance [6] what was out of the scope of this experiment.

V. Conclusion

For the first time, sensitivity analysis of the *in-situ* over-temperature calibration was performed for the multiline TRL and the transfer TMR implemented in the advanced SiGe BiCMOS process up to 110 GHz. The obtained results demonstrated that temperature variations of the electrical characteristics of load and line standards lead to different calibration residual errors depending on the calibration method used.

For the considered experimental setup, we found that the multiline TRL calibration method was less sensitive to temperature. However, the worst-case error bound for both methods were three times less than the typical drift of the measurement setup. Therefore, complicated and time-consuming experiments for characterization of the temperature coefficients of custom calibration standards are not required. Extracted C_{BE} of a test HBT proved this statement. Results of this investigation significantly simplify implementation of the advanced *in-situ* calibration methods into the conventional characterization workflow of advanced SiGe devices.

References

[1] N. Derrier, A. Rumiantsev, and D. Celi, "State-of-the-art and future perspectives in calibration and de-embedding techniques for characterization of advanced SiGe HBTs featuring sub-THz fT/fMAX," in *Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), 2012. IEEE*, Portland, OR, 2012, pp. 92-99.

[2] A. Rumiantsev, G. Fisher, and R. Doerner, "Sensitivity analysis of wafer-level over-temperature RF calibration," in *Microwave Measurement Symposium (ARFTG)-Fall, 80th*, San Diego, CA, USA, 2012, pp. 1-3.

[3] R. B. Marks and D. F. Williams, "Characteristic impedance determination using propagation constant measurement," *IEEE Microwave and Guided Wave Letters,* vol. 1, pp. 141-143, June 1991.

[4] D. F. Williams and R. B. Marks, "Transmission line capacitance measurement," *Microwave and Guided Wave Letters, IEEE,* vol. 1, pp. 243-245, 1991.

[5] H. Rucker, B. Heinemann, W. Winkler, *et al.*, "A 0.13 um SiGe BiCMOS technology featuring ft/ fmax of 240/330 GHz and gate delays below 3 ps," *Solid-State Circuits, IEEE Journal of,* vol. 45, pp. 1678-1686, 2010.

[6] A. Rumiantsev, "On-Wafer calibration techniques enabling accurate characterization of high-performance silicon devices at the mm-wave range and beyond," Fakultät für Maschinenbau, Elektrotechnik und Wirtschaftsingenieurwesen, BTU Cottbus, Cottbus, 2014.